REMARKS

Request for Continued Examination

Applicant respectfully requests continued examination of the above-indicated application as per 37 CFR 1.114.

Claims 1-7 and 9-18 are rejected under 35 USC 103a as being unpatentable over Kaku et al., US Patent 6,414,932, in view of Kato et al., US Patent 6,775,217

Applicant has amended claim 1 to include all the limitations of claim 16. Claim 16 is correspondingly cancelled. Applicant asserts that claim 16 should not have been found rejected under 35 USC 103a as being unpatentable over Kaku et al. and Kato et al. because neither reference teaches the limitations of claim 16. The Examiner stated in the Final Office action mailed 08/01/2006, "Regarding claim 16, Kaku et al. teaches the high-speed optical recording apparatus wherein the delay cells are a plurality of serially connected inverters or buffers (the differential amplifiers of figure 5 serve this purpose as is explained in column 6, lines 1-10), the fine delay chain further comprising a multiplexer for selecting the write signal from a plurality of outputs of the inverters or buffers (the selection method given in column 4, lines 41-53 serves the same purpose)."

However, applicant respectfully points out that Kaku et al. cannot teach anything about the delay cells of the fine delay chain because Kaku et al. does not teach a fine delay chain. Figure 5 of Kaku et al. also does not show the differential amplifiers relied upon by the Examiner. Applicant assumes the Examiner meant the differential amplifiers of figure 5 of Kato et al (US 6,775,217), and notes the Examiner stated in the advisory action "regarding the argument that Kaku et al. does not specifically teach a fine delay chain, Kato et al. is relied upon for this feature." However, Kato et al. do not teach the required features because figure 5 of Kato et al. has nothing to do with the fine delay 324. In particular, Kato et al. states in col 6 starting at line 1, "Fig5 is a block diagram and waveform diagram of the ring oscillator comprising multi-phase clock synthesizer 320 of Fig.3." That is, figure 5 shows the

implementation and waveform diagram of the multi-phase clock synthesizer 320, which is not part of the fine delay 324. Kato et al. does not teach or suggest that the circuit structure of figure 5 could be utilized to implement the fine delay 324. The applicant respectfully asserts that the Examiner is unfairly relying on hindsight to observe that figure 5 of Kato et al. could be utilized to implement functionality of Fig.3 of the present invention. However, without the benefit of the disclosure and teachings of the present invention, there is nothing in Kato et al. to suggest that the fine delay 324 should or even could be implemented with serially connected inverts or buffers, and further comprising a multiplexer for selecting the write signal from the outputs of the inverters or buffers.

In the present invention currently amended claim 1 (including all limitations from cancelled claim 16), the required limitations include that "the delay cells are a plurality of serially connected inverters or buffers, the fine delay chain further comprising a multiplexer for selecting the write signal from a plurality of outputs of the inverters or buffers." Applicant notes that earlier in claim 1, the term "the delay cells" is clearly directed at the fine delay chain. In particular, claim 1 states, "the fine delay chain having a plurality of serially connected delay cells, each delay cell delaying the first delay signal by a predetermined period". For at least this reason, applicant asserts that currently amended claim 1 should not be found unpatentable over Kaku et al. and Kato et al. because neither reference teaches "the delay cells are a plurality of serially connected inverters or buffers, the fine delay chain further comprising a multiplexer for selecting the write signal from a plurality of outputs of the inverters or buffers." Specifically, applicant points out that figure 5 of Kato et al. does not teach or suggest this structure for use in the fine delay 324. Reconsideration of claim 1 is respectfully requested. Claims 4-15, and 17-18 are dependent upon claim 1 and should therefore be found allowable for at least the same reasons.

Claim 8 is rejected under 35 USC 103a as being unpatentable over Kaku et al., US Patent 6,414,932, in view of Kato et al., US Patent 6,775,217 as applied to claim 3 above, and further in view of Chung et al., US Patent 4,873,680

As stated above, claim 8 is dependent on claim 1, which is believed by applicant

to be allowable over the cited references. Therefore, claim 8 should also be found allowable over said cited references. Reconsideration of claim 8 is respectfully requested.

New Claims

Applicant has added new claims 19-40. No new matter is entered. In particular, claims 20-35 are based directly on original claims 2-15 and 17-18, respectively. Independent claim 19 is based on original claim 1 with limitations similar to original claim 16 but being more structurally specific of the fine delay chain. Fig.3 and the corresponding description in paragraph [0023] of the present invention fully support the claimed structure as stated in claim 19. Claim 36 is fully supported as shown in Fig.1, Fig.3 and described in paragraph [0023]. Note is made that the fine delay chain 18 as shown in Fig.1 and Fig.3 delays S1 by an amount of delay solely determined according to the fine delay parameter outputted by the delay adjustment state machine 20. Claim 37 is supported in the same figures as there is no clock signal being connected to the fine delay chain, and the operation of the fine delay chain 18 as described in paragraph [0023] does not require the use of a clock signal to delay the first delay signal to generate the write signal. Claims 38 and 39 are both supported from limitations present in original claim 16. Claim 40 is a combination of a subset of the limitations of claim 19 and claim 37. Specifically, claim 40 omits the multiplexer limitation of claim 19, but incorporates the no clock signal required limitation of claim 37. Claim 40 is supported for the same reasons as stated above for claims 19 and 37.

Concerning the patentability of claim 19 with respect to the cited references above, applicant points out that neither Kaku et al. nor Kata et al. teach or suggest that the fine delay chain be implemented in the same manner as is claimed in the present invention claim 19. Specifically, "the fine delay chain comprising a plurality of serially connected delay cells, an output of each delay cell thereby delaying the first delay signal by a predetermined period corresponding to a number of previous delay cells in the fine delay chain; and the fine delay chain further comprising a multiplexer having inputs coupled to the outputs of the delay cells, a selecting end coupled to the fine delay parameter, and an output end being coupled to the write signal, the

multiplexer for generating the write signal being one of the outputs of the delay cells as selected according to the fine delay parameter." (claim 19)

The benefit of the claimed fine delay chain structure is described in paragraph [0010] of the present invention stating, "The high-speed optical recording apparatus contains a fine delay chain, which includes a plurality of delay cells in serial connection, for providing fine delays that the high-speed optical recording apparatus needs. As each delay cell delays the input signal with a predetermined time period and because the predetermined time is an extremely short time period, the high-speed optical recoding apparatus according to the claimed invention has satisfactory resolution of fine delays with the delay cells properly adjusted, to solve the above mentioned problem." Because the cited references do not teach or suggest the claimed structure, and because the benefit of the claimed structure is clearly disclosed in the present invention, applicant asserts that said limitations should be given patentable weight as claimed. For at least the reason that the structure of the fine delay chain is different, applicant asserts that claim 19 should be found allowable over the cited references of Kato et al. and Kaku et al. Claims 20-39 are dependent upon claim 19 and therefore should be found allowable for at least the same reason.

Concerning the patentability of claims 36, 37, and 40 applicant points out that in figure 3 of the disclosure of Kato et al., the fine delay 324 delays the output of the rough delay 322 according to the $4f_{EFM0-7}$ clock signal outputted by the multi-phase clock synthesizer in addition to the N2 output of the write strategy delay table 350. This is described in col 5 starting at line 1 by Kato et al. to allow the fine delay 324 to generate delays in increments of 1/32T. Such operation is not equivalent to the "fine delay chain is for delaying the first delay signal only according to the fine delay parameter so as to generate the write signal", as is claimed in claim 36. It is also not equivalent to "the fine delay chain is not connected to and does not utilize a clock signal for delaying the first delay signal to generate the write signal", as is claimed in claims 37 and 40. For at least these reasons, applicant asserts claims 36, 37, and 40 should be found allowable with respect to the cited references.

Sincerely yours,

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